What is claimed is:

[Claim 1] 1. A semiconductor structure, comprising:

first and second source/drain regions;

a channel region disposed between the first and second source/drain regions;

a buried well region in physical contact with the channel region; and

a buried barrier region being disposed between the buried well region and the first source/drain region and being disposed between the buried well region and the second source/drain region,

wherein the buried barrier region is adapted for preventing leakage current between the buried well region and the first source/drain region and between the buried well region and the second source/drain region.

[Claim 2] 2. The semiconductor structure of claim 1, further comprising:

a gate region; and

a gate dielectric layer disposed between and electrically insulating the gate region and the channel region from each other.

[Claim 3] 3. The semiconductor structure of claim 2, wherein the gate region comprises polysilicon.

[Claim 4] 4. The semiconductor structure of claim 1, wherein the buried barrier region comprises silicon dioxide.

[Claim 5]

5. The semiconductor structure of claim 1, wherein the first and second source/drain regions are heavily doped.

[Claim 6] 6. The semiconductor structure of claim 1, wherein the buried well region is heavily doped.

[Claim 7] 7. A method for forming a semiconductor structure, the method comprising the steps of:

(a) providing a semiconductor substrate covered on top with a mandrel layer;
(b) etching a trench through the mandrel layer and into the substrate;
(c) forming a buried barrier region on a side wall of the trench, wherein the buried barrier region is in direct physical contact with both the substrate and the mandrel layer;
(d) forming a buried well region and a channel region in the trench, wherein the channel region is on top of the buried well region; and
(e) forming first and second source/drain regions,
wherein the channel region is disposed between the first and second source/drain regions, and
wherein the buried barrier region is disposed between the buried well region and the first source/drain region and is disposed between the buried well region and the second source/drain region.

[Claim 8] 8. The method of claim 7, wherein the buried well region is heavily doped.

[Claim 9] 9. The method of claim 7, wherein the buried barrier region is adapted for essentially eliminating junction capacitance (i) between the buried well region and the first source/drain region and (ii) between the buried well region and the second source/drain region.

[Claim 10] 10. The method of claim 7, wherein the buried barrier region is adapted for essentially eliminating leakage current (i) between the buried well region and the first source/drain region and (ii) between the buried well region and the second source/drain region.

[Claim 11] 11. The method of claim 7, wherein the step of forming the buried barrier region comprises the steps of:

depositing a buried barrier layer on side and bottom walls of the trench such that the buried barrier layer is in direct physical contact with both the substrate and the mandrel layer; and

etching away a portion of the buried barrier layer at the bottom wall of the trench so as to form the buried barrier region from the buried barrier layer.

[Claim 12] 12. The method of claim 7, wherein the buried barrier region comprises silicon dioxide.

[Claim 13] 13. The method of claim 7, wherein the step of forming the buried well region and the channel region comprises the steps of:

depositing a semiconductor material in the trench so as to form an under-gate region such that the buried barrier region is completely buried in the under-gate region; and

doping a portion of the under-gate region which is surrounded by the buried barrier region,

wherein the doped portion of the under-gate region comprises the buried well region, and

wherein an undoped portion of the under-gate region on top of the buried well region comprises the channel region.

[Claim 14] 14. The method of claim 13, wherein the semiconductor material is deposited in the trench by growing silicon epitaxially.

[Claim 15] 15. The method of claim 13, wherein the doped portion of the under-gate region is doped by ion implantation.

[Claim 16] 16. The method of claim 7, further comprising the steps of:

forming a gate dielectric layer on top of the channel region; and then
forming a gate region on top of the gate dielectric layer before the step of forming first and second source/drain regions,
wherein the gate region is electrically insulated from the channel region by the gate dielectric layer.

[Claim 17]

17. A method for forming a semiconductor structure, the method comprising the steps of:
(a) providing a semiconductor substrate covered on top with a mandrel layer;
(b) etching a trench through the mandrel layer and into the substrate;
(c) forming a buried barrier region on a side wall of the trench, wherein the buried barrier region is in direct physical contact with both the substrate and the mandrel layer;
(d) depositing a semiconductor material in the trench so as to form an under-gate region such that the buried barrier region is completely buried in the under-gate region;
(e) forming a gate spacer region on side walls of the trench;
(f) doping via the trench a portion of the under-gate region which is surrounded by the buried barrier region, wherein the doped portion of the under-gate region comprises a buried well region, and wherein an undoped portion of the under-gate region on top of the buried well region comprises a channel region;
(g) forming a gate dielectric layer on top of the channel region;
(h) forming a gate region on top of the gate dielectric layer, wherein the gate region is electrically insulated from the channel region by the gate dielectric layer; and
(i) forming first and second source/drain regions in the substrate,
wherein the channel region is disposed between the first and second source/drain regions,
wherein the buried barrier region is disposed between the buried well region and the first source/drain region and is disposed between the buried well region and the second source/drain region, and
wherein the buried barrier region is adapted for preventing leakage current between the buried well region and the first source/drain region and between the buried well region and the second source/drain region.

[Claim 18] 18. The method of claim 17, wherein the step of forming the buried barrier region comprises the steps of:

depositing a buried barrier layer on side and bottom walls of the trench such that the buried barrier layer is in direct physical contact with both the substrate and the mandrel layer; and

etching away a portion of the buried barrier layer at the bottom wall of the trench so as to form the buried barrier region from the buried barrier layer.

[Claim 19] 19. The method of claim 18, wherein the buried barrier layer comprises silicon dioxide.

[Claim 20] 20. The method of claim 17, wherein the step of forming the gate spacer region comprises the steps of:

forming a gate spacer layer on side and bottom walls of the trench; and

removing a portion of the gate spacer layer on the bottom wall of the trench so as to form the gate spacer region from the gate spacer layer.

[Claim 21]

21. A method for forming a semiconductor structure, the method comprising the steps of:
(a) providing a silicon-on-insulator (SOI) substrate covered on top with a mandrel layer, wherein the SOI substrate includes (i) an upper semiconductor layer, (ii) a lower semiconductor layer, and (iii) an electrical insulator layer sandwiched between the upper and lower semiconductor layers;
(b) etching a trench through the mandrel layer and into the SOI substrate such that the lower semiconductor layer is exposed to the atmosphere at a bottom wall of the trench;
(c) forming a buried barrier region on a side wall of the trench, wherein the buried barrier region is in direct physical contact with both the SOI substrate and the mandrel layer;
(d) forming a buried well region and a channel region in the trench, wherein the channel region is on top of the buried well region; and
(e) forming first and second source/drain regions,
wherein the channel region is disposed between the first and second source/drain regions,
wherein the buried barrier region is disposed between the buried well region and the first source/drain region and is disposed between the buried well region and the second source/drain region.

[Claim 22] 22. The method of claim 21, wherein the buried well region is heavily doped.

[Claim 23] 23. The method of claim 21, wherein the buried barrier region is adapted for essentially eliminating junction capacitance (i) between the buried well region and the first source/drain region and (ii) between the buried well region and the second source/drain region.

[Claim 24] 24. The method of claim 21, wherein the buried barrier region is adapted for essentially eliminating leakage current (i) between the buried well region and the first source/drain region and (ii) between the buried well region and the second source/drain region.

[Claim 25] 25. The method of claim 21, wherein the step of forming the buried barrier region comprises the steps of:

depositing a buried barrier layer on side and bottom walls of the trench such that the buried barrier layer is in direct physical contact with both the substrate and the mandrel layer; and

etching away a portion of the buried barrier layer at the bottom wall of the trench so as to form the buried barrier region from the buried barrier layer.

[Claim 26] 26. The method of claim 21, wherein the buried barrier region comprises silicon dioxide.

[Claim 27] 27. The method of claim 21, wherein the step of forming the buried well region and the channel region comprises the steps of:

depositing a semiconductor material in the trench so as to form an under-gate region such that the buried barrier region is completely buried in the under-gate region; and

doping a portion of the under-gate region which is surrounded by the buried barrier region,

wherein the doped portion of the under-gate region comprises the buried well region, and

wherein an undoped portion of the under-gate region on top of the buried well region comprises the channel region.

[Claim 28] 28. The method of claim 27, wherein the semiconductor material is deposited in the trench by growing silicon epitaxially.

[Claim 29] 29. The method of claim 27, wherein the doped portion of the under-gate region is doped by ion implantation.

[Claim 30] 30. The method of claim 21, further comprising the steps of:

forming a gate dielectric layer on top of the channel region; and then
forming a gate region on top of the gate dielectric layer before the step of forming first and second source/drain regions,
wherein the gate region is electrically insulated from the channel region by the gate dielectric layer.